Docket No.: SYCS-035

Application No.: 09/872263

REMARKS

Upon entry of this paper, claims 1-25 are pending. Applicant has added new independent claims 24 and 25. Claims 1 and 22 have been amended. No claims have been cancelled. No new matter has been added.

Indication of Allowable Subject Matter

Applicant appreciates the Examiner's indication that claims 7-20 and 23 contain allowable subject matter and are allowed.

Summary of New Claims

Applicant has added new claims 24 and 25 which are system claims corresponding to the previously allowed method claims 7 and 23. Applicant respectfully suggests that new claims 24 and 25 are allowable on the same basis.

Claim Rejections Pursuant to 35 U.S.C. §102(b)

The Examiner rejected claims 1-6 and 21-22 pursuant to 35. U.S.C. 102(b) as being anticipated by Ganmukhi et al (U.S. Patent No. 5, 953, 314, hereafter "Ganmukhi"). In light of the amendments above and the arguments below, the Applicant respectfully traverses each of these rejections.

Summary of Claimed Invention

The claimed invention discusses systems and methods of providing reset logic in high availability computer systems. The illustrative embodiment of the present invention uses probability theory in combination with redundant processors and components to ensure system availability. Detected errors are verified and malfunctioning processors or components are then changed to a reset state that functionally removes them from the system. Detected errors which can not be verified result in the processor or component that incorrectly detected the error being placed in a reset state. The use of redundant components and processors enable standby processors to be activated to take the place of reset processors quickly enough to maintain system availability.

Docket No.: SYCS-035

Application No.: 09/872263

Summary of Claim Amendments

Applicant has amended claims 1 and 22 to specify that the original error in the other processor that is detected by the system control processor in the active state is verified by the system control processor in the standby state prior to the two system control processors altering the activation state of the other processor in which the error was detected.

Summary of Ganmukhi

Ganmukhi discusses a control processor switchover for a telecommunications switch. Multiple control processor cards are deployed in the switch along with multiple switch fabric cards. One of the control processor cards is designated as the active card and one of the control processor cards is designated as a standby. Similarly, one of the switch fabric cards is designated as an active card and one of the switch fabric cards is designated as a standby card. An error in either the active control processor card or active switch fabric card is handled by switching over to the appropriate standby card. Each of the standby cards has the same capabilities as the corresponding active card. The use of a redundant control processor card in addition to the use of a redundant fabric switch card provides a system that is more robust than those systems deploying only a redundant switch fabric card.

Argument

As set forth in MPEP § 2131, "[a] claim is anticipated [under 102(b)]only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." The Applicants respectfully submit that, under this standard, Ganmukhi does not disclose every element of independent claims 1, 21 and 22, and therefore does not anticipate claims 1, 21 and 22 or the claims which are dependent on claim 1 (claims 2-6).

Specifically, Ganmukhi does not disclose the limitation in claim 1 of verifying the detected error in the other processor using the system control processor set to a standby state. Additionally, Ganmukhi does not disclose the limitation in claim 1 that the alteration of the

activation state of the other processor in which the error was detected takes place after the verification by the system control processor in the standby state. Similarly, Ganmukhi does not disclose the limitation in claim 21 of the verification of the error by the system control processor in the standby activation state. Likewise, the limitation of claim 22 of the verification of the error by the standby system control processor and alteration of the activation state following that verification are also absent from Ganmukhi.

The claimed invention provides a verification and decision on error events in a system. Once an error is detected an immediate attempt is made to verify the error using the standby system control processor. Either the error is immediately verified (in which case the faulty component has its activation state reset) or the error determination by the active system control processor is found to be faulty in the event the error cannot be verified by the standby system control processor (which results in the activation state of the active system control processor being changed). In contrast, in Ganmukhi, the standby system control processor is not involved in system operations until such time as the active system control processor has been found to fail. While the standby system control processor in Ganmukhi has the same capabilities as the active system control processor, it does not actively operate until such time as a failure has already been detected in the active system control processor ("When a switch is powered-ON or reset, only one of the control processor cards 12, 14 can become active. The non-active control processor card is considered to be in standby mode. An active control processor card is distinguished from a standby control processor card by having exclusive control over central resources and internal resources", see col 3, lines 13-18).

Ganmukhi is directed towards the replacement or switchover of a failed system control processor card without disruption of data flow, see col. 3, lines 38-42. The health of the active control processor card is monitored by the standby control processor card through the mechanism of the active control processor card periodically sending signals to the standby control processor card. If the signal fails to arrive at the designated time, the standby control processor sends a termination signal which starts a change in the respective activation states of the control processor cards (see col 3, line 62 – col 4, line 6). This is quite different from standby system control processor of the claimed invention taking part in a process that verifies an error in another processor that was originally detected by the active system control processor.

Ganmukhi simply fails to discuss the standby control processor taking an active part in the verification process of an error originally detected by the active system control processor. Accordingly, Applicant requests that the rejections directed towards claims 1-6 and 21-22 be withdrawn and the claims allowed.

Docket No.: SYCS-035

Application No.: 09/872263

CONCLUSION

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

Applicant believes no fee is due with this statement. However, if a fee is due, please charge our Deposit Account No. 12-0080, under Order No. SYCS-035 from which the undersigned is authorized to draw.

Dated: June 18, 2004

Respectfully submitted,

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